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IMPACT OF CURRENT LEAKAGE IN HIGH SPEED VLSI SYSTEM USING LOW POWER MANAGEMENT TECHNIQUE: AN ANALYSIS

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Abstract

This article explores the experimental analysis of current leakage in high speed VLSI system using low power management technique. As we know that theHigh-Speed and Low-power are the major challenges for today's electronics industries. Power dissipation is an important consideration in terms of Speed/Performance and space for VLSI Chip design. Power management techniques are generally used to designing low power circuits and systems. This thesis presents the various VLSI Design Methodologies for high Speed and Low power management techniques that can meet future challenges to designs low power high speed/performance circuits, algorithm level design. It also describes the many issues regarding circuits design at architectural, logic and device levels and presents various techniques to overcome difficulties. Present generation of electronic design scenario demands low power architectures. In earlier days, power was secondary as the field was premature and main concerns of design engineers were size, throughput and cost. However trade off exists between the metrics namely, size, throughput, cost and power according to the famous design metric competition theory of VLSI systems wherein improving one deteriorates the other metric. The performance of any circuit is affected greatly by its components.

1. OVERVIEW

Low power plays a very important role and in today's current trends of VLSI. There are appraisal techniques and extension circuits employed in low power VLSI designs. Power dissipation has main thought as performance and area. Because of higher quality, decreasing power consumption and power management on chip are the key challenges right down to 100nm. Reducing package price and battery life is a very important issue in optimization of power. Leakage current plays a very important role in power management and conjointly low power is a major drawback in high performance digital and microchip system. Leakage current is a primary issue in total power dissipation of integrated circuits. For victorious chip it solely wants low power consumption, calculation of power dissipation[1-7].

This research discusses about future challenges that must be to design and use for low power circuits spans a wide range from device or method level to formula level. Analog and mixed signal integrated circuits play a significant role in designing integrated circuits. It comprises of both analog and digital signals in a single semiconductor die. It is commonly used as a communication interface among the digital and real world signals.

The designing of analog circuitry part is found to be critical because of the immense complexity and size perception. Furthermore, the miniaturization in the circuit design provides special emphasis to the production of the System on Chip (SOC) and is dominated by the effects of nanoscale elements. Due to the effect of ever-growing demand and the advancements in terms of miniaturization, the designers are facing scaling issues and also there is an exponential growth in terms of complexity, which influences on the productivity and performance of the analog and mixed mode systems.

Furthermore, minimizing the energy consumption rate in modern processors can extend the lifespan of the semiconductor devices and battery, especially in portable devices. The advancement in VLSI technologies has made the digital and analog circuits to scale down into nanometer range, which results in exponential increase of sub threshold leakage current, threshold voltage and power consumption. The concern in terms of power consumption has increased rapidly due to the design complexity and the structure density. Hence, there exists a requirement of an accurate power modeling technique to address the issues of nanometer processing technologies. Different modeling techniques have been discussed in This research and the process of Input Vector Control (IVC) is found to be a better alternative in achieving the low power consumption.

Applying effective optimization technique to calculate their design parameters is observed to be a better possible method for reducing power consumption in the system. In this research, a novel technique comprising gravitational search algorithm is developed to optimize the power of the circuit. Arithmetic Logic Unit (ALU) is designed for 16 bit to evaluate the performance of the system. Furthermore, comparison study of other techniques with GSA elevates the design of ALU in terms of Leakage Power and the time to reach the optimal solution.

2. LEAKAGE REDUCTION TECHNIQUES

- **MTCMOS**

The low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. Low, normal and high threshold voltage transistors are

used to design a CMOS circuit in this technique. With the scaling of CMOS technology, Supply and threshold voltages are reduced. Sub threshold leakage current increases exponentially with lowering of threshold voltage.

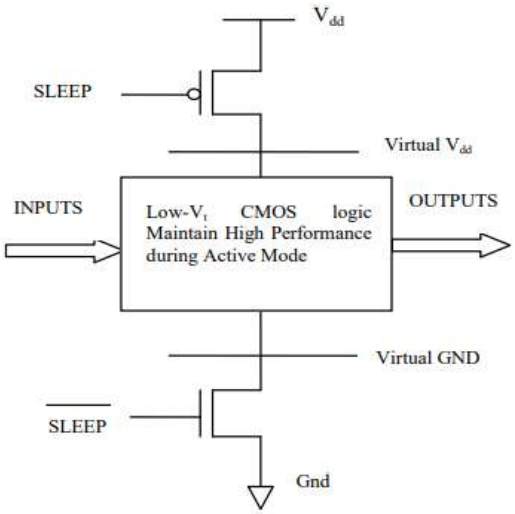

Figure 1: General MTCMOS circuit architecture

Multi-threshold CMOS (MTCMOS) is a design technique in which high threshold sleep transistors are connected between the logic circuit and power or ground, thus creating a virtual supply rail or virtual ground rail, respectively. The low threshold voltage transistors which have high performance are used to reduce the propagation delay time in the critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path. MTCMOS circuit technology which satisfies both the requirements of lowering the threshold voltage to obtain high speed and reducing standby current to have low power. The two main features of this technique are employing two different threshold voltages on a single circuit and having two operational modes active & sleep for efficient power management.

Dual V_t

Dual threshold voltage technique also uses two threshold voltages as in the case of MTCMOS. Here, high threshold voltage (HTV) is assigned to transistors of some gates in the non-critical paths while specifying the low-threshold voltage for the gates in the critical path. In this technique, no additional transistors are required as in the case of multithreshold voltage technique. Reduction of static power is achieved while maintaining the same performance as single threshold voltage circuit. Care should be taken while designing, is that if all the transistors

in the non-critical paths are assigned with HVT, non-critical path may become a new critical path with a larger path delay than the original one, deteriorating the speed of the circuit.

Leakage control transistor (Lector) technique

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This states that "a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one off transistor path.

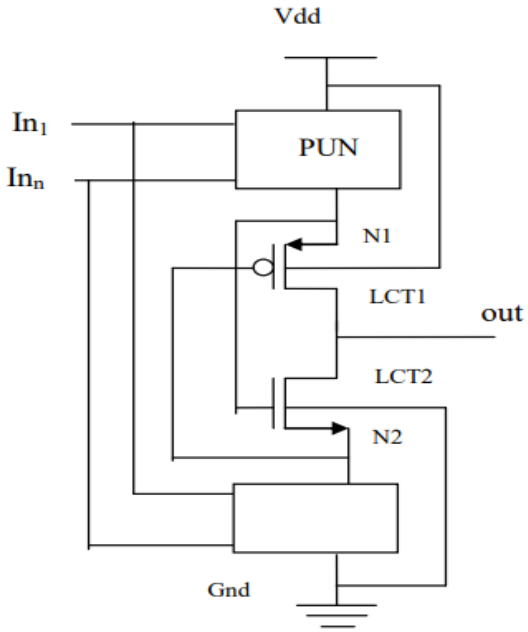

Figure 2: Lector CMOS Gate

The LECTOR implementation involves the addition of two LCTS for each gate between the supply and ground path. The general architecture of the LECTOR technique is shown in Fig.3.

Proposed Method 1

This is a modified structure of MTCMOS technique. In this structure, the NMOS HVT sleep transistor is arranged as a stack of two transistors with width twice that of original one. A state is far less leaky with more than one OFF transistor compared to a state with only one OFF transistor in the path. This modified method reduces the leakage power to a great extent compared to that of existing.

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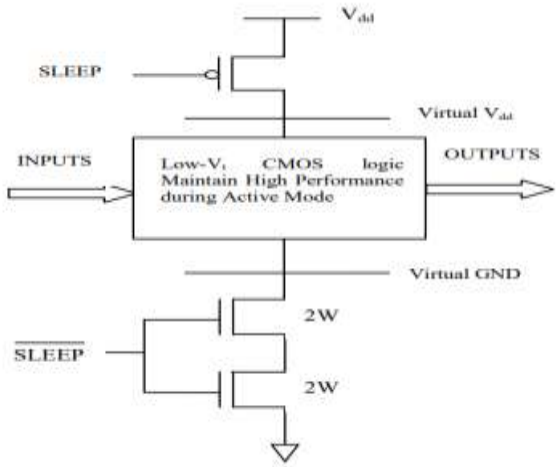

Figure 3: logic diagram of proposed method 1

Proposed Method 2

It is an improvised structure of existing dual-Vt technique. An NMOS transistor is kept between ground and logic circuit.

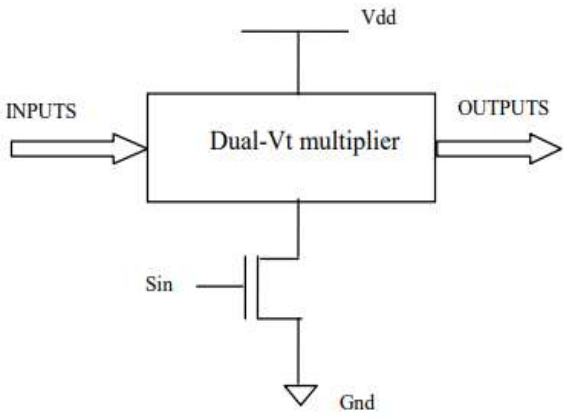

Figure 4: Logic Diagram Proposed Method 2

In active mode, NMOS will be kept ON allowing the circuit to operate normally. In inactive mode NMOS will be kept OFF which provides high resistance path between power supply and ground. The NMOS is kept ON/OFF by means of controlling input Sin.

Proposed method 3

In the proposed design, the critical path blocks in an 8 bit carry-save multiplier are replaced with LCT blocks and other non-critical path blocks are assigned with high threshold voltage. A PMOS transistor is kept over the developed logic which intern cut-off the power supply to the logic block in inactive mode.

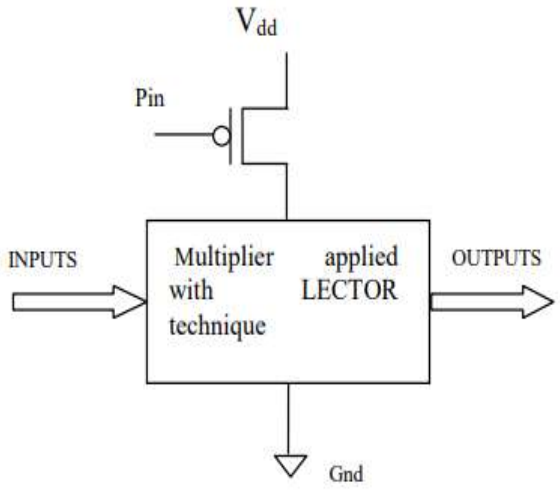

Figure 5.Logic Diagram Proposed Method 3

3. EXPERIMENTAL ANALYSIS

In This research an 8X8 multiplier is designed using leakage power reduction techniques like MTCMOS, DUAL-Vt, LECTOR and proposed methods. These designs are simulated using Cadence virtuoso tool in 90nm technology. Table.1 shows the simulation results of all the above techniques in terms of average power, Delay and static power. Figure [6], [7] and [8] represents the comparison of above techniques in terms of average power, delay and static power. From the simulation results, proposed methods give 99.99%, 99.02% and 99.98% of reduction in static power respectively.

Table 1: Simulation result of 8x8 multiplier

Method	Average power (μw)	Delay (ps)	Static power(w)
Basic multiplier	62.75	91.84	3.3263 e-6
Multi-threshold	28.98	274.76	3.7387 e-11
Dual-threshold	20.71	119.80	7.1452e-7
LECTOR	28.27	130.85	6.3806e-6
Proposed method1	26.89	346.94	8.4968e-12
Proposed method2	19.84	145.15	3.2453e-8
Proposed method3	16.51	137.50	4.4948e-10

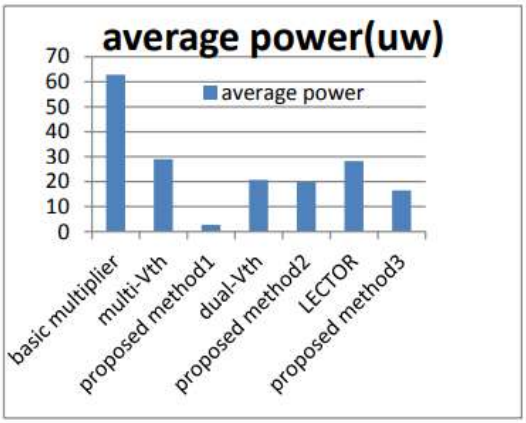

Figure 6: Comparing Average Power of above techniques

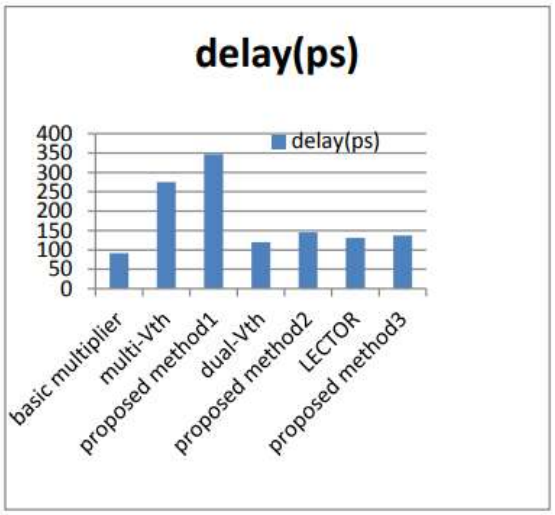

Figure 7: Comparing average Power of above technique

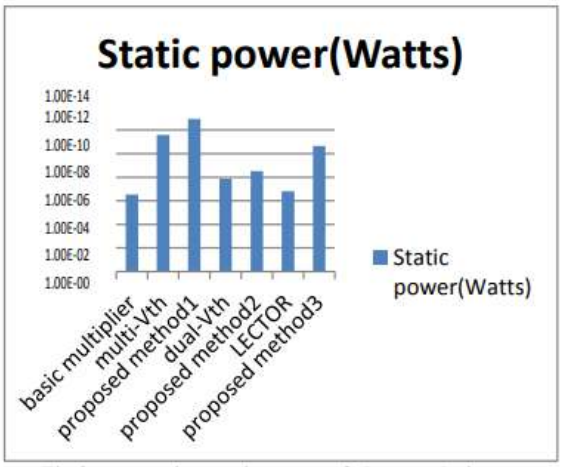

Figure 8: Comparing Static Power of above techniques

4. CONCLUSION

Optimization of the design is accomplished by compromising designissues as well as components. With the ever-shrinking technology, especially below 90 nm, power dissipation and its management has been critical for the design engineers. Significance of optimization has been understood from the fact that how important it is to have an extended battery life and at the same time reducing the package cost. This research presents a literature review upon the strategies and methodologies in designing low power VLSI systems. CMOS technology is the key element in the development of VLSI systems since it consumes less power.

Power optimization has become an overridden concern in deep submicron CMOS technologies. Due to shrink in the size of device, reduction in power consumption and over all power management on the chip is the key challenges. For many designs power optimization is important in order to reduce package cost and to extend battery life. In power optimization leakage also plays a very important role because it has significant fraction in the total power dissipation of VLSI circuits. This paper aims to elaborate the developments and advancements in the area of power optimization of CMOS circuits in deep submicron region.

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